## ABSTRACT

The present invention relates to a method for manufacturing a wafer level chip scale package structure including the following steps. After providing a glass substrate and a wafer comprising a plurality of chips, the active surface of the wafer is connected to the top surface of the glass substrate. The wafer is connected with the glass substrate through either bumps or pads thereon. After drilling the glass substrate to form a plurality of through holes, a plating process is performed to form a plurality of via plugs in the through holes. Afterwards, a singulation step is performed and a plurality of chip scale package structures is obtained.